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Fault Coverage Testing on the ISCAS'89 S1423 Sequential Circuit using Scan Based Design and Synopsis Tetramax

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ABSTRACT

We tested the ISCAS'89 S1423 series with a scan design method, both non-scan, full-scan, and partial-scan, but for the partial-scan, the method we propose uses a structured random approach. The purpose of this study is to determine the evaluation and performance with the best computational time with the proposed method to produce high fault coverage results. Testing the ISCAS'89 S1423 circuit in the form of verilog was carried out using tetramax synopsis, the partial-scan test requires a strategy in determining the flip flop to be used as a scannable flip flop, the test results using the full scan method produce 100% test coverage and fault coverage, but this method provides gate overhead loss of 24.06% and slower chip performance. To reduce the gate overhead loss, a partial-scan method will be applied with the approach of choosing from 74 DFF which will be used as scannable flip flops, the test with the best results we did through the 37 DFF approach with the highest input obtained test coverage of 98.17% and fault coverage 96.76% with 171.11 CPU Time with gate overhead reduced by 12.03%. The next approach with the best results with the approach of 50 DFF highest output plus DFF which is not self-loop obtained test coverage of 99.24% and fault coverage of 98.47% with gate overhead successfully reduced by 16.26% with CPU Time 43.39.

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1. INTRODUCTION

In design for testability (DFT), both a combinational and a sequential circuits requires a test so that the circuit becomes reliable. There are several test methods to test a circuit, but testing sequential circuits with scan-based design methods is preferred [1] however, a different approach in finding fault coverage is carried out by [2], where fault detection techniques and statistical verification frameworks are used in estimating the true FC, When a circuit is not tested in the final stages of chip manufacturing, what can happen is that the fault coverage of the circuit cannot be verified, in other words a circuit at the final stage of chip manufacturing must be tested. This test can be performed using various methods or approaches to obtain high fault-coverage results. But oftentimes when the chip does not get good quality, the chip becomes unreliable. The full-scan method always gets test coverage with high results because it converted to combined test generation but this method leaves a problem with the hardware size and gate overhead which results in high chip manufacturing costs. One of the methods proposed to reduce the size of the hardware and gate overhead in a chip design is to test with the partial-scan method, in this method, a sequential sequence will be given a scan chain, the idea of a scan chain is to add additional inputs on the flip flop, namely standard input or scan data input, a control signal is used to select a standard input or scan data input, then a scan chain will be formed by connecting the output of a flip flop to the scan data input of another flip flop. For each clock cycle, the data enters the scan chain at data_in and ends at the scan chain data_out. However, the strategy of selecting the flip flop that will be used as a scannable flip flop is a separate strategy, the purpose of selecting flip flop that will be used as a scannable flip flop is to get the highest possible test coverage with some of the flip flops that will be used as a scannable flip flop, unlike full-scan which by makes the entire flip flop to be scannable. In this study, the authors tried to

test the fault coverage of the ISCAS'89 S1423 circuit in the form of a Verilog file. The ISCAS'89 S1423 circuit consists of 17 inputs, 5 outputs, 74 type D flipflops, 167 inverters and 490 gates (197 AND + 64 NAND + 137 OR +92 NOR) and 10 sequential-depths [3]. The purpose of testing the ISCAS'89 S1423 circuit is to determine the highest possible fault coverage and test coverage in the S1423 circuit and to obtain the best approach method to reduce gate overhead for this type of partial-scan test.

2. RESEARCH METHOD

In the chip manufacturing process, there are several stages, including chemical, metallurgical and optical processes. If the resulting chip production is 75% good, then the rest is chip failure, therefore the testing process is needed. Design for Testability (DFT) refers to design practices where several questions such as whether all faults on the chip can be ascertained, whether the manufacturing process time can be more efficient and whether the execution time of chip testing can be more economical. In addition, various improvements of test coverage to achieve high fault coverage with as few test patterns as possible as proposed by [4] with Test Point Insertion. One other problem is delay fault testing, where [5] proposes a DFT technique to reduce the number of logic gates used as test points in order to reduce the overhead area and the number of additional inputs. One of the DFT methods is the structured method, the scan-based method is the structured method, where this method is an alternative to the ad-hoc method which has weaknesses along with the size and complexity of the growing digital system. The test method for the ISCAS'89 S1423 circuit in this study was carried out using a structured method because the circuit has a large number of flip flops, the test of this circuit is carried out in several stages, first the circuit will be downloaded in verilog form, the second is modifying the circuit in tetramax design vision so that it can be read properly, thirdly modifying the circuit by adding a scan-chain, after that the circuit is ready to be tested using a scan-based design method, which is full-scan and partial-scan. The initial S1423 circuit is shown in **Fig. 1** and one of the flip flops is shown in **Fig. 2**.

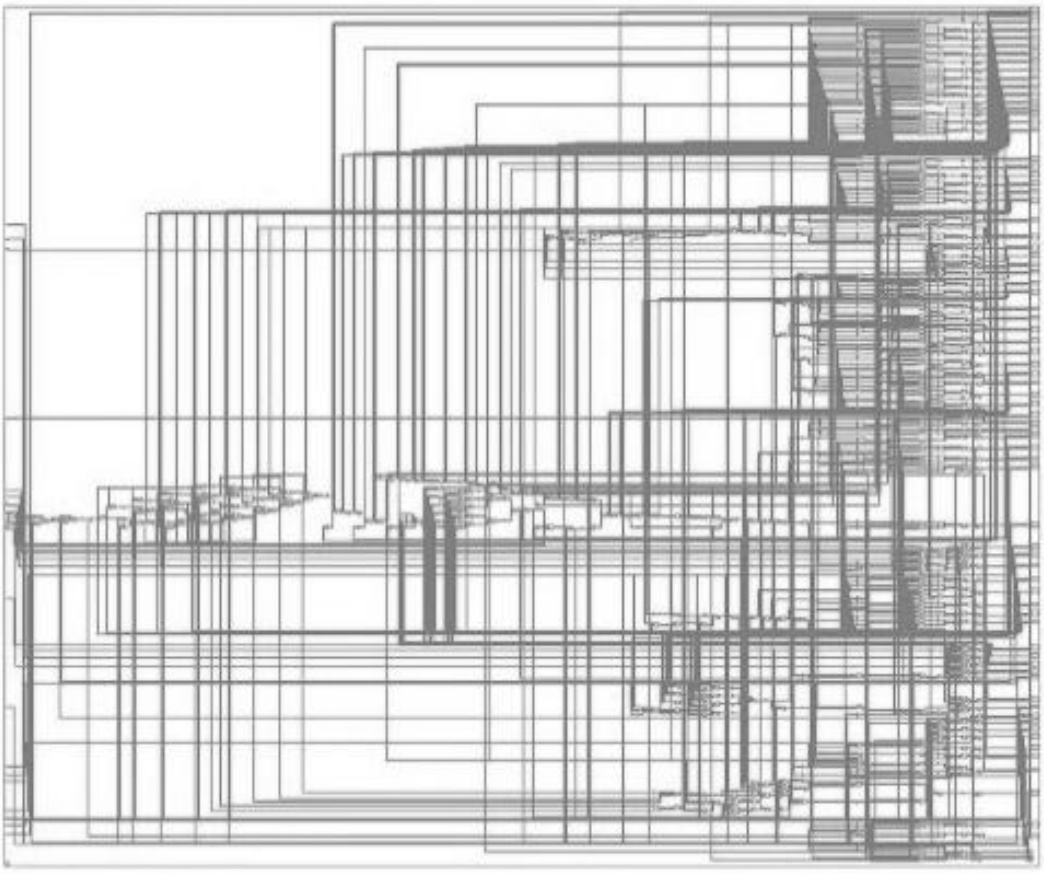

Fig. 1. Initial S1423 circuit before optimization in Synopsis Tetramax

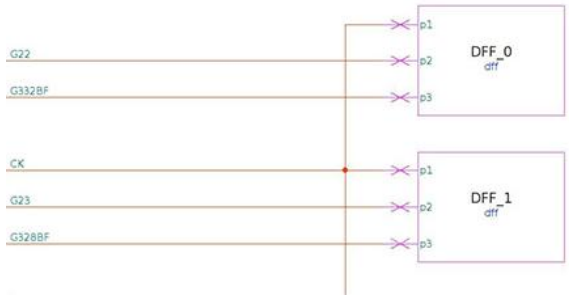

Fig. 2. One of the S1423 Flip flops before the optimization in synopsis Tetramax.

2.1. Circuit Optimization

In general, circuits that have not been optimized will give low test coverage results, this is due to among other things, the presence of a redundant fault or component in the circuit and the entire flip flop is made non-scannable flip flop, it is common practice to find undetectable and redundant faults in a synchronous sequential circuit is to use a circuit test pattern generator or in some cases using the W-method [6] to predict how often transition faults occur and what percentage of fault coverage is generated. in this case, it is enough to modify the flip flop circuit on the verilog by change the flip flop writing format on the S1423.v circuit from dff file_name (CK, Q, D) to FD1 file_name (.D (input), .CP (clock), .Q (output)) formats.

Circuit after optimization is shown in **Fig. 3** and the flip flop after optimization shown in **Fig. 4**, we can see the change in the shape of the circuit and one of the flip flops that has been optimized and further modify it by adding scan-chain.

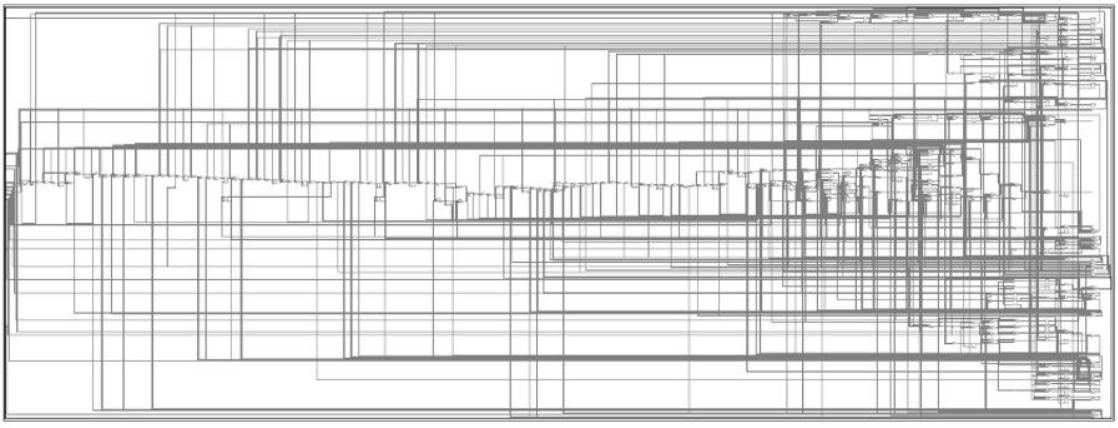

Fig. 3. S1423 circuit after optimization

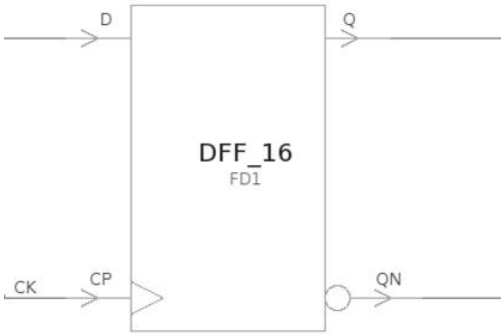

Fig. 4. One of the flip flops in the S1423 circuit after optimization

2.2. Modification process by adding a scan-chain

In the process of testing the circuit in tetramax with the full-scan and partial-scan methods, the optimized circuit needs to be added with a scan-chain. The idea of a scan-chain is basically adding additional inputs to the flip flop, standard input and scan input data as in **Fig. 5.** The control signal or scan_enable is used to select the input standard for a scan of the input data as, then a scan-chain is formed by connecting the output of one flip flop to the scan data input of another flip flop [7] as shown in **Fig. 6.** The end of this scan-chain is the final circuit that will be tested as shown in **Fig. 7**. For each clock cycle, data enters the scan-chain at data_in and ends at scan chain data_out, the behavior of this scan chain is controlled by the scan_en signal as shown in the following figures.

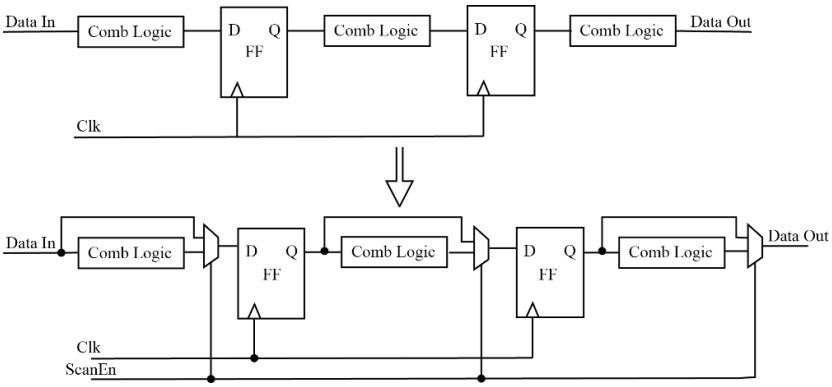

Fig. 5. Scan chain idea

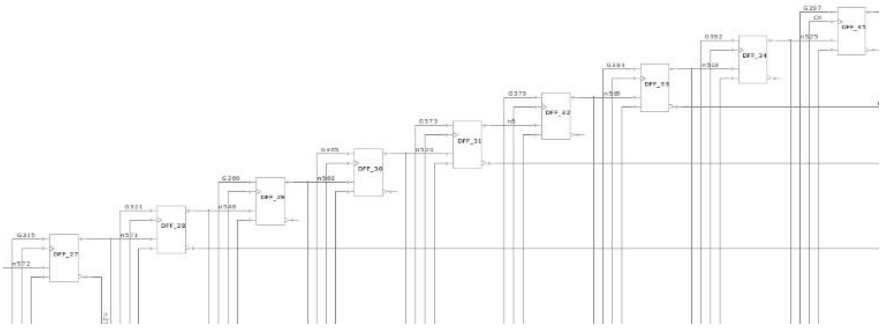

Fig. 6. Flip flops after adding scan chain

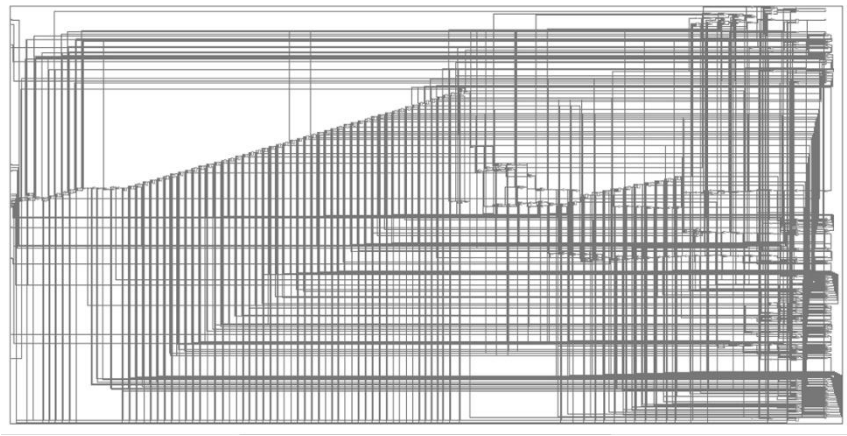

Fig. 7. S1423 circuit after is given the scan-chain process

In the scan chain process, there are potential failures caused among others by stuck-at-faults and timing faults among others is excessive test power consumption, to overcome this some authors propose scan-chain architecture to reduce test power consumption such as [8]. An indication of the failure of the scan chain is a very low or zero yield, even today where modern chips are based on nanometer technology, some researchers propose a low cost method for stuck-at-fault problems where the method of diagnosing the problem is claimed to be effective, low complexity, solution suitable as Dounavi et al proposed [9], the above hardware-assisted diagnostic method is claimed to be better than the simulation diagnostic method, but due to the considerable overhead, the method is said to be not accepted in practical designs, therefore Ahlawat et al proposed the hardware-assisted method following the previous method and the proposed design has less gate overhead in terms of area and performance [10]. In today's world where the chip size is in nanometers, scan-chain faults are analyzed using Neural Networks such as [11] to produce a better diagnosis.

2.3. Circuit testing with non-scan and full-scan methods

The non-scan method is a test method in which none of the flip flops are made scannable flip flops, because no flip flops are scannable flip flops, it will result in low fault coverage and test coverage. Testing this method is only a comparison to the full-scan method and partial-scan. The full scan method is a method in which all flip flops are scannable flip flops, the results of this test will produce high test coverage and fault coverage, but as explained earlier this method leaves a problem namely hardware size and gate overhead which leads to manufacturing costs as the chip gets bigger.

2.4. Circuit testing with the partial-scan method

By testing with the partial-scan method, we can reduce the amount of hardware used which results in a smaller gate overhead or chip size. This is because in testing using the partial-scan method, the number of flip flops that are converted into scannable flip flops is only partial or incomplete. To find out which flip flop will be used as a scannable flip flop, we can analyze the circuit with several approaches, in this case we use FSM based [12]. We proposed custom approach with the largest number of inputs and outputs of selected flip flops to achieve high result of fault coverage and test coverage as in **Fig. 8**, Table 1 and Table 2.

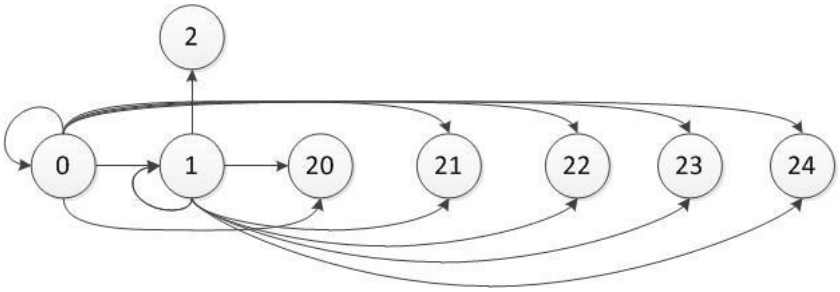

Fig. 8. Pseudo S-graph example for the highest number of input and output

From **Fig. 8** we can make the matrix for the highest number of input and output as seen in Table 1.

Table 1. Pseudo s-graph matrix example of highest input from **Fig. 8.**

DFF	**Number of flip flops**							
	0	1	2	20	21	22	23	24
0	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	1	1
2	0	0	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0
23	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0
Total Input	1	2	1	2	2	2	2	2

As we can see in Table 1. DFF0 has 1 input, DFF1 has 2 inputs, DFF2 has 1 input, DFF20 has 2 inputs and so on, and for Table 2 we can see that DFF0 and DFF1 has 7 output and for the rest is 0. The S-graph for the S1423 circuit is too difficult and complicated to see with the naked eye, therefore we create an s-graph matrix and sort it from the highest number of inputs and outputs to the lowest as seen in Table 2.

Table 2. Pseudo S-graph matrix example of highest output from **Fig. 8**.

DFF	Number of flip flops								Total Output
	0	1	2	20	21	22	23	24	
0	1	1	0	1	1	1	1	1	7
1	0	1	1	1	1	1	1	1	7
2	0	0	0	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0	0
23	0	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0	0

As we can see in Table 1, DFF0 has 1 input, DFF1 has 2 inputs, DFF2 has 1 input, DFF20 has 2 inputs and so on, and for Table 2 we can see that DFF0 and DFF1 has 7 output and for the rest is 0. The S-graph for the S1423 circuit is too difficult and complicated to see with the naked eye, therefore we create an s-graph matrix and sort it from the highest number to the lowest of inputs and outputs as shown in Table 3 and Table 4.

Table 3. Highest to lowest number of inputs for the S1423 circuit

No	DFF	Hi-Low (input)	15	29	44	31	32	28	47	41	17	63	43	8
1	46	52	16	36	42	32	17	27	48	21	16	64	1	6
2	47	52	17	35	42	33	71	27	49	3	16	65	0	5
3	45	52	18	37	42	34	12	26	50	20	15	66	69	3
4	48	52	19	61	41	35	11	25	51	2	15	67	70	3
5	53	47	20	16	33	36	10	24	52	63	9	68	72	2
6	54	47	21	15	33	37	9	23	53	62	9	69	68	2
7	55	47	22	26	31	38	8	22	54	60	9	70	67	2
8	56	47	23	27	31	39	7	21	55	59	9	71	66	2
9	52	47	24	28	31	40	73	20	56	58	9	72	65	2
10	31	45	25	14	31	41	6	19	57	57	9	73	13	1
11	39	45	26	19	29	42	24	19	58	51	9	74	64	0
12	38	45	27	33	29	43	23	18	59	50	9			
13	40	45	28	25	29	44	5	18	60	49	9			
14	30	45	29	34	29	45	4	17	61	44	9			
			30	18	28	46	22	17	62	42	9			

Table 4. Highest to lowest number of output for the S1423 circuit

No	DFF	Hi-Low (output)
1	68	56
2	20	49
3	21	48
4	22	47
5	23	46
6	52	46
7	42	46
8	54	46
9	53	46
10	56	46
11	55	46
12	63	46
13	62	46
14	24	46
15	2	43
16	3	42
17	70	42
18	4	41
19	5	40
20	6	39
21	7	38
22	8	37
23	9	36
24	12	36
25	10	35
26	69	35
27	11	34
28	47	26
29	46	26
30	45	26
31	51	26
32	50	26
33	49	26
34	48	26
35	17	25
36	41	25
37	18	24
38	16	23
39	60	23
40	58	23
41	57	23
42	59	23
43	19	23
44	44	23
45	14	22
46	61	22
47	15	21
48	36	13
49	37	12
50	31	10
51	26	9
52	27	9
53	25	8
54	28	8
55	39	7
56	34	7
57	32	7
58	0	7
59	40	6
60	1	6
61	13	5
62	64	3
63	29	3
64	72	2
65	67	2
66	66	2
67	65	2
68	43	2
69	38	2
70	35	2
71	33	2
72	30	2
73	71	0
74	73	0

The purpose of selecting flip flops to be scannable flip flops is to reduce gate overhead and performance with the expectation that fault coverage and test coverage are close to 100% with as few flip flops as possible to choose from, the approach in choosing a flip flop that will be used as a scannable flip flop from Table 3 and Table 4 above is as follows.

1. As S1423 circuits has 74 DFF, first approach to select the flip flops will be half of all the DFF which is 37 DFF with all possible combination
    a. 37 DFF with the highest number of inputs
    b. 37 DFF with the lowest number of inputs
    c. 37 DFF with the highest number of output
    d. 37 DFF with the lowest number of output
2. If the results of fault coverage and test coverage are not close to 99%, then we increase the selection of scannable flip flops from 37 DFF to a random number that we choose 50 DFF with the hope that as little as possible the selected flip flop can produce fault coverage and test coverage close to 99, 99%, if it is close to 99,99%, it can be said that the circuit is sufficient to represent fault coverage and test coverage even though it is not as good as a full scan, which is 100%.
3. Also another technique to reduce overhead, we need to eliminate paths that have long cycles, namely DFFs that have self-loop, therefore we will choose DFFs that are not self-looping, and of all the flip flops in the S1423 circuit almost all of them are self-loop except DFF71, DFF73, DFF64, DFF25, if not self-loop then it can be said that the flip flop path has a short cycle so it can be selected also we will add to the selection only 50 scannable DFF because 50 DFF is more and represents than 37 DFF.

From all the approaches above, we can see in detail in Table 5.

Table 5. The result of selecting the DFF to be used as a scannable flip flop

Selection of Scannable flip flop	Flip Flop (DFF) number
37 DFF with the highest number of inputs	46, 47, 45, 48, 53, 54, 55, 56, 52, 31, 39, 38, 40, 30, 29, 36, 35, 37, 61, 16, 15, 26, 27, 28, 14, 19, 33, 25, 34, 18, 32, 17, 71, 12, 11, 10, 9
37 DFF with the lowest number of inputs	8, 7, 73, 6, 24, 23, 5, 4, 22, 41, 21, 3, 20, 2, 63, 62, 60, 59, 58, 57, 51, 50, 49, 44, 42, 43, 1, 0, 69, 70, 72, 68, 67, 66, 65, 13, 64
37 DFF with the highest number of output	68, 20, 21, 22, 23, 52, 42, 54, 53, 56, 55, 63, 62, 24, 2, 3, 70, 4, 5, 6, 7, 8, 9, 12, 10, 69, 11, 47, 46, 45, 51, 50, 49, 48, 17, 41, 18
37 DFF with the lowest number of output	16, 60, 58, 57, 59, 19, 44, 14, 61, 15, 36, 37, 31, 26, 27, 25, 28, 39, 34, 32, 0, 40, 1, 13, 64, 29, 72, 67, 66, 65, 43, 38, 35, 33, 30, 71, 73
50 DFF with the highest number of inputs (+ DFF not self-looping)	46, 47, 45, 48, 53, 54, 55, 56, 52, 31, 39, 38, 40, 30, 29, 36, 35, 37, 61, 16, 15, 26, 27, 28, 14, 19, 33, 25, 34, 18, 32, 17, 71, 12, 11, 10, 9, 8, 7, 73, 6, 24, 23, 5, 4, 22, 41, 21, 3, 20 (25, 64, 71, 73)
50 DFF with the lowest number of inputs (+ DFF not self-looping)	28, 14, 19, 33, 25, 34, 18, 32, 17, 71, 12, 11, 10, 9, 8, 7, 73, 6, 24, 23, 5, 4, 22, 41, 21, 3, 20, 2, 63, 62, 60, 59, 58, 57, 51, 50, 49, 44, 42, 43, 1, 0, 69, 70, 72, 68, 67, 66, 65, 13, 64, (25, 64, 71, 73)
50 DFF with the highest number of output (+ DFF not self-looping)	68, 20, 21, 22, 23, 52, 42, 54, 53, 56, 55, 63, 62, 24, 2, 3, 70, 4, 5, 6, 7, 8, 9, 12, 10, 69, 11, 47, 46, 45, 51, 50, 49, 48, 17, 41, 18, 16, 60, 58, 57, 59, 19, 44, 14, 61, 15, 36, 37, 31(25, 64, 71, 73)
50 DFF with the lowest number of output (+ DFF not self-looping)	12, 10, 69, 11, 47, 46, 45, 51, 49, 50, 48, 17, 41, 18, 16, 60, 58, 57, 59, 19, 44, 14, 61, 15, 36, 37, 31, 26, 27, 25, 28, 39, 34, 32, 0, 40, 1, 13, 64, 29, 72, 67, 66, 65, 43, 38, 35, 33, 30, 71, 73, (25, 64, 71, 73)

3. RESULT AND DISCUSSION

Based on the entire research method and the table above, we tested using tetramax with the results of the coverage and fault coverage tests as seen in Table 6.

Table 6. Non-scan method S1423 circuit test results

Testing Parameters	Non-scan method test results
Detected Fault	8
Possibly detected	0
Undetectable	0
ATPG Untestable	2618
Not Detected	0
Total Faults	2626
Test Coverage	0.30 %
CPU Time	0.00
Fault Coverage	0.3 %

From the results of Table 6, it can be seen that the number of detected faults is very small and the ATPG untestable is very large and the test coverage and fault coverage is very small, this has been explained earlier because the circuit that has not been optimized will produce fault coverage and test coverage is very small because there are redundants and the entire flip flop is made non-scannable. The full-scan test result can be seen in Table 7.

Table 7. Test results of the S1423 circuit with the full-scan method

Testing Parameters	Full-scan method test results
Detected Fault	2626
Possibly detected	0
Undetectable	0
ATPG Untestable	0
Not Detected	0
Total Faults	2626
Test Coverage	100 %
CPU Time	0.03
Fault Coverage	100 %

The full scan method results high test coverage and fault coverage, but as explained earlier this method leaves a problem, namely hardware size and gate overhead which leads to manufacturing costs as the chip gets bigger. In overcoming this problem, in recent years with the increasing need for chips, especially those used in the IoT field, optimization of the layout design chip is needed in order to reduce the cost of the increasingly large chip as done by [13].

The method we propose to overcome this is to use the partial-scan method and the test result with 37 DFF can be seen in Table 8, and 50 DFF in Table 9 respectively.

Table 8. Partial-scan test results with 37 flip flop data selection

Testing Parameters	**Partial-Scan Test Results**			
	37 highest input	37 lowest input	37 highest output	37 lowest output
Detected Fault	2541	2449	2491	2525
Possibly Detected	74	74	74	74
Undetectable	0	0	0	0
ATPG Untestable	0	40	29	0
Not Detected	11	63	32	27
Total Faults	2626	2626	2626	2626
Test Coverage	98.17%	94.67%	96.27%	97.56%
CPU Time	171.11	1261.42	543.13	588.12
Fault Coverage	96.76%	93.25%	94.85	96.15%

From Table 8, it is obtained that the results of the highest test coverage and fault coverage are at the highest 37 flip flop input approach with the results of 98.17% for test coverage and 96.76% for fault coverage. This result is quite good, but not too good with the results we expect, which is close to 99.99% with the remaining 37 DFF that have not been used as scannable flip flops.

Table 9. Partial-scan test results with data selection of 50 flip flops

Testing Parameters	**Partial-Scan Test Results**			
	50 highest input (+ not self loop DFF)	50 lowest input (+ not self loop DFF)	50 highest output (+ not self loop DFF)	50 lowest output (+ not self loop DFF)
Detected Fault	2577	2569	2586	2561
Possibly Detected	46	52	40	48
Undetectable	0	0	0	0
ATPG Untestable	0	0	0	0
Not Detected	3	5	0	17
Total Faults	2626	2626	2626	2626
Test Coverage	99.01%	98.82%	99.24%	98.44%
CPU Time	16.42	241.22	43.39	395.27
Fault Coverage	98.13%	97.82%	98.47%	97.52

Table 9 show the results of the highest test coverage and fault coverage are obtained on the 50 DFF approach with the highest output + not self loop DFF, namely 99.24% for test coverage and 98.47% for fault coverage, these results are quite good compared to the previous approach and are close to 99%.

4. CONCLUSION

Among the testing methods on the scan-based design method, the partial-scan method is popular because it can reduce gate overhead and increase performance, but in this method we must use a sequential ATPG program, one of which is provided by Tetramax, in this method requires a strategy in determining the flipflop to be used. used as scannable flip flops, especially in sequential circuits with a large number of flip flops, some of the commonly used techniques are Minimum Feedback Vertex Set (MFVS) namely finding the smallest set of vertice, and in this case we tested the S1423 circuit with a random approach selected flip flops with the best results resulted in fault coverage of 98.47% and test coverage of 99.24% with CPU time of 43.39 with a 50 scannable DFF + not self loop DFF approach and this partial-scan approach was able to reduce gateoverhead by 16.26%.

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